Intel® Centrino™ Mobile Technology Platform Overview

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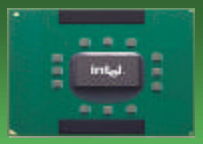
Agenda

- Overview
- Intel® Pentium® M processor
  - Micro-op Fusion
  - Advanced Branch Prediction
  - Hardware Stack Manager
  - Cache Architecture
  - Enhanced Intel Speedstep® Technology
  - Compatibility
- Software optimizations
  - Performance
  - Connectivity
  - Power Management

Intel® Centrino™ Mobile Technology



Intel® Pentium® M processor

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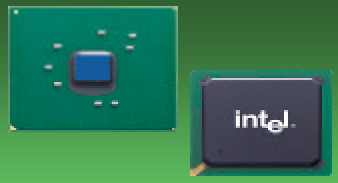

Intel® 855 chipset family

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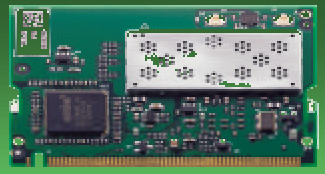


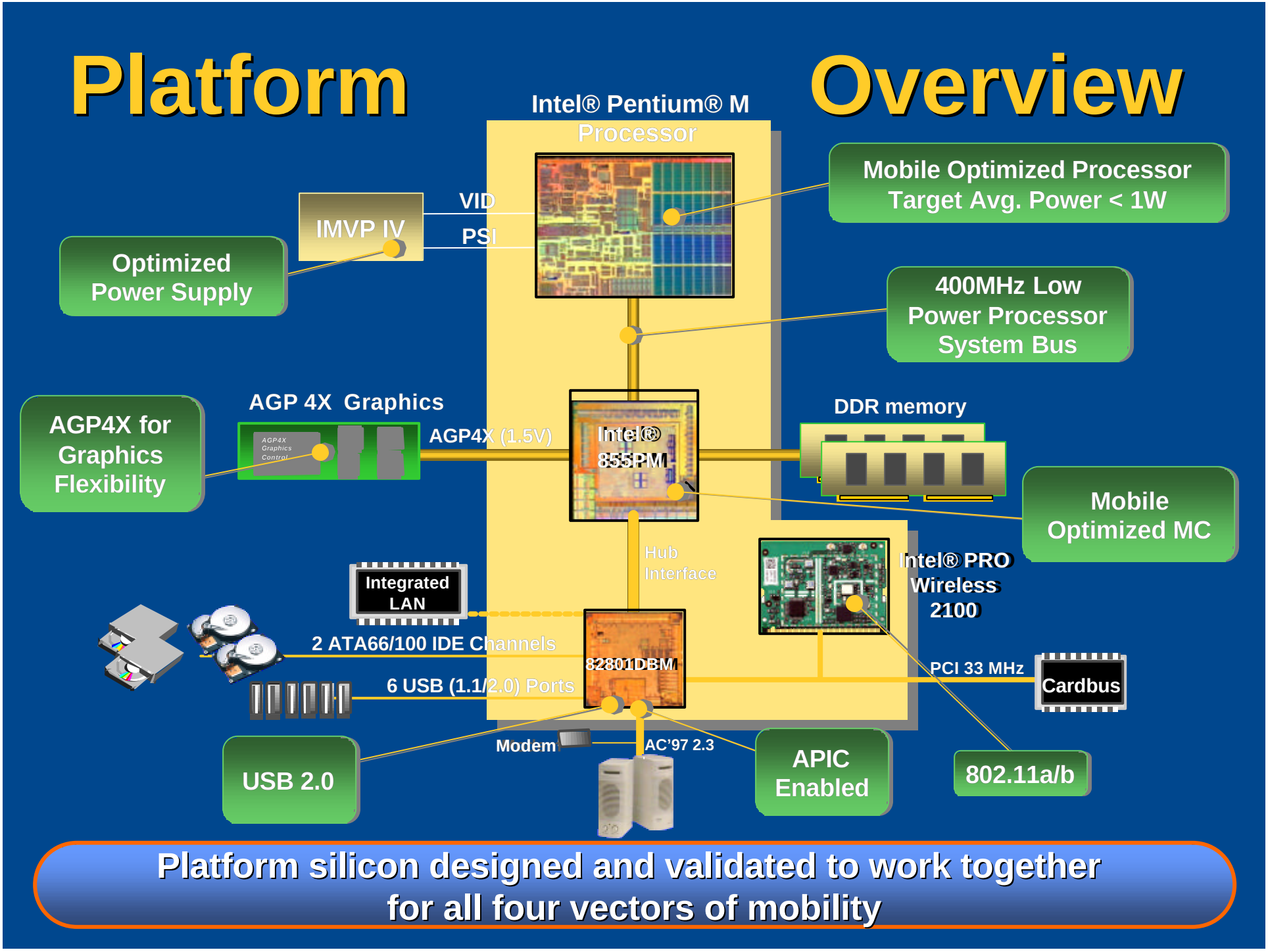
Intel® PRO/Wireless 2100 network connection

*Images not to scale

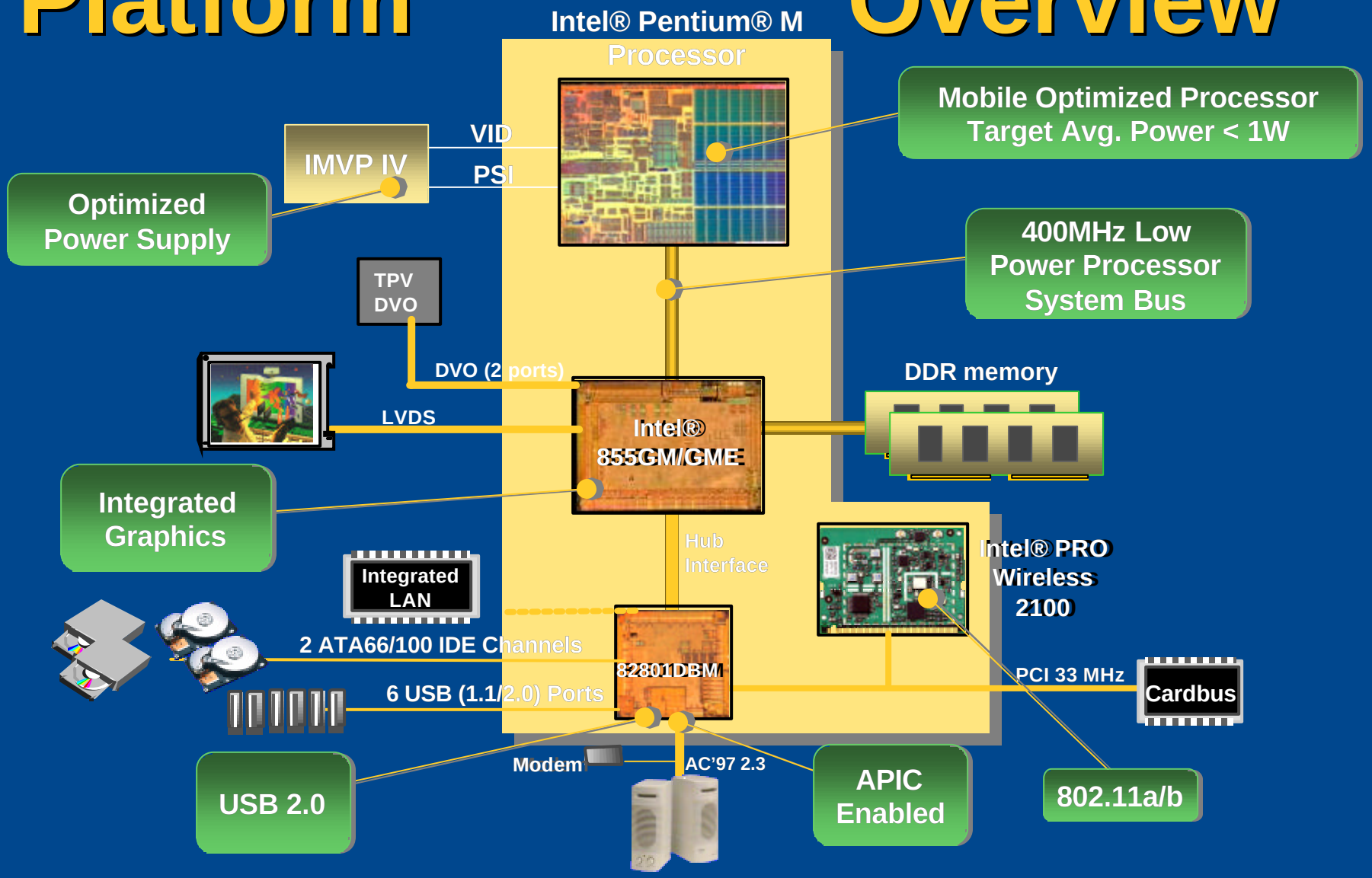
- Four Vectors of Mobility
  - Performance
  - Battery Life
  - Connectivity
  - Form-factor

Bottoms-up Mobile-specific design

Platform Overview



Platform Overview

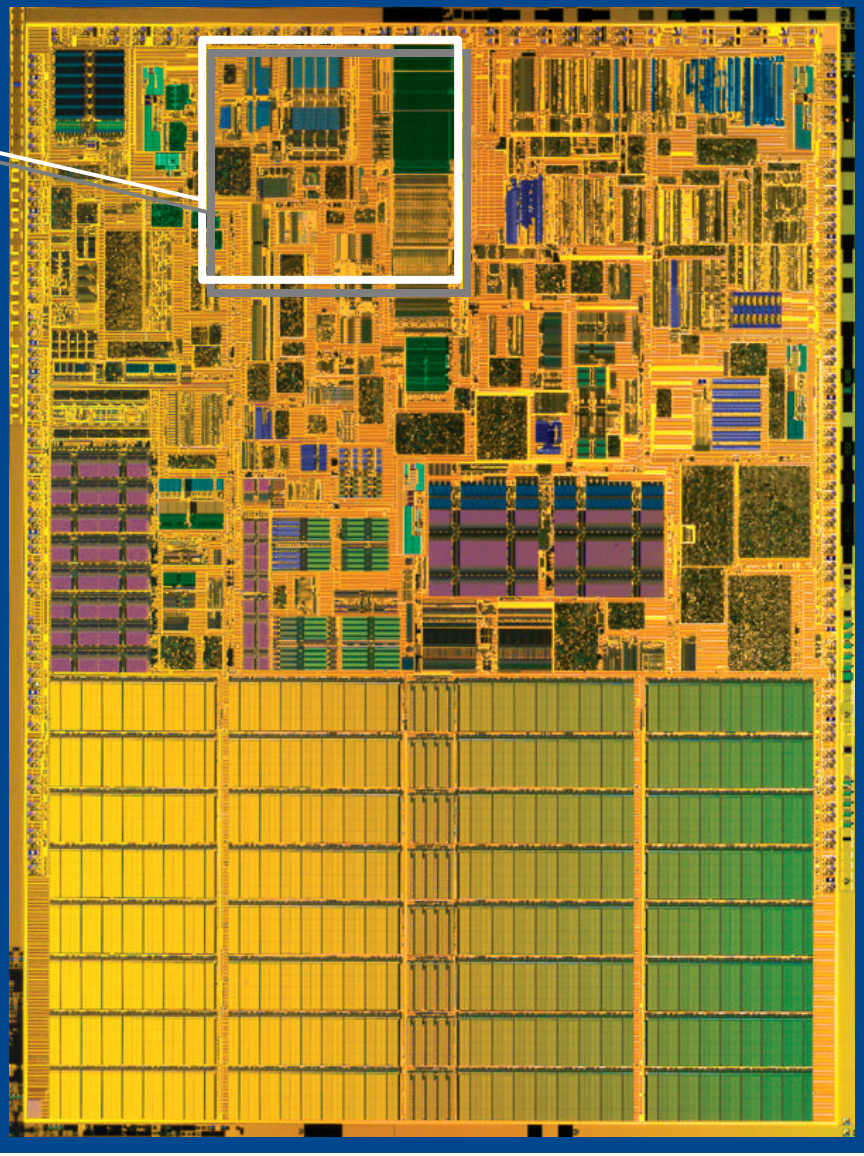


Integrated graphics with Intel® 855GM designed and validated for high performance with space and power savings

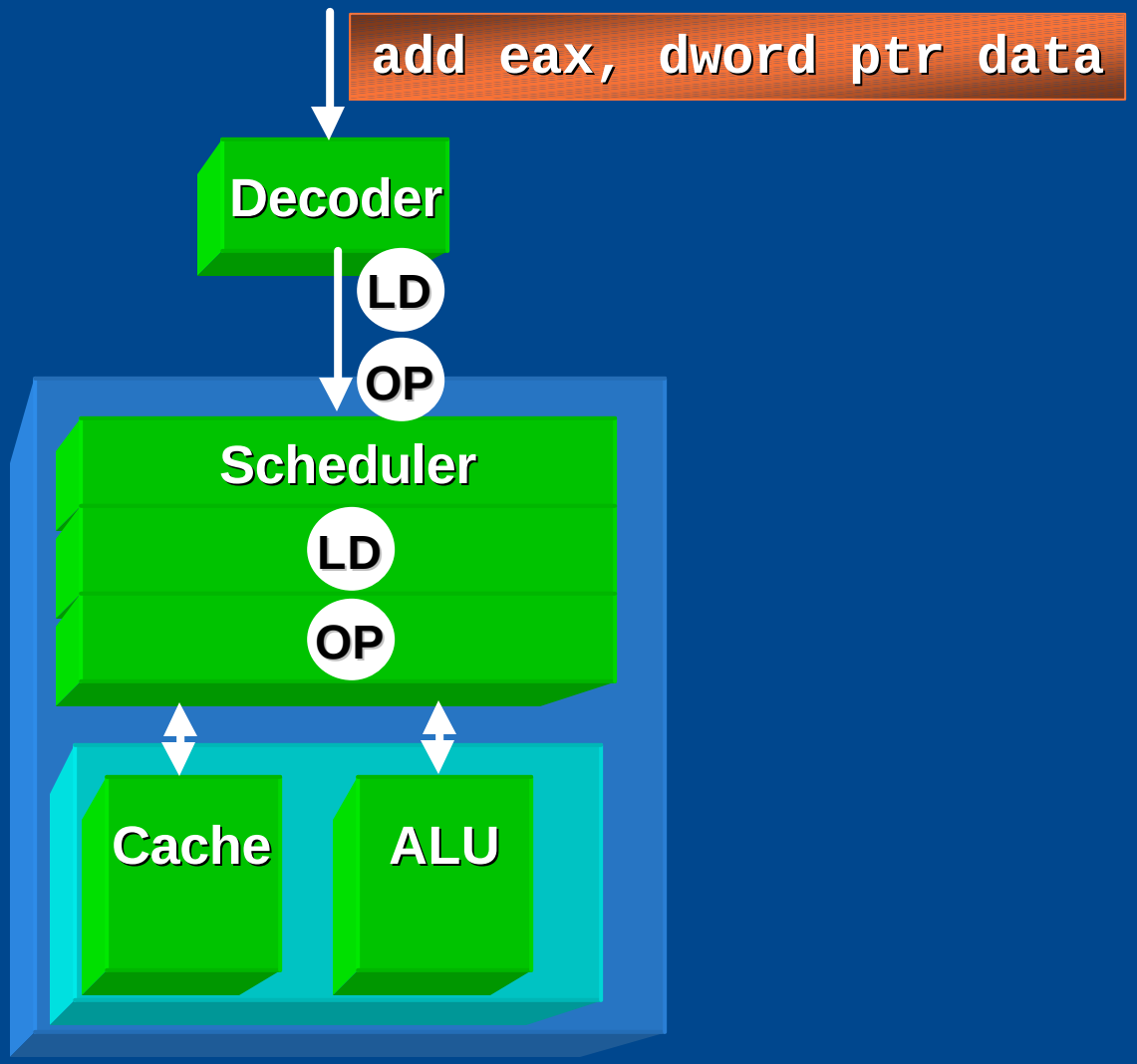
Intel Pentium M Processor

77 million transistors

Micro-Ops Fusion

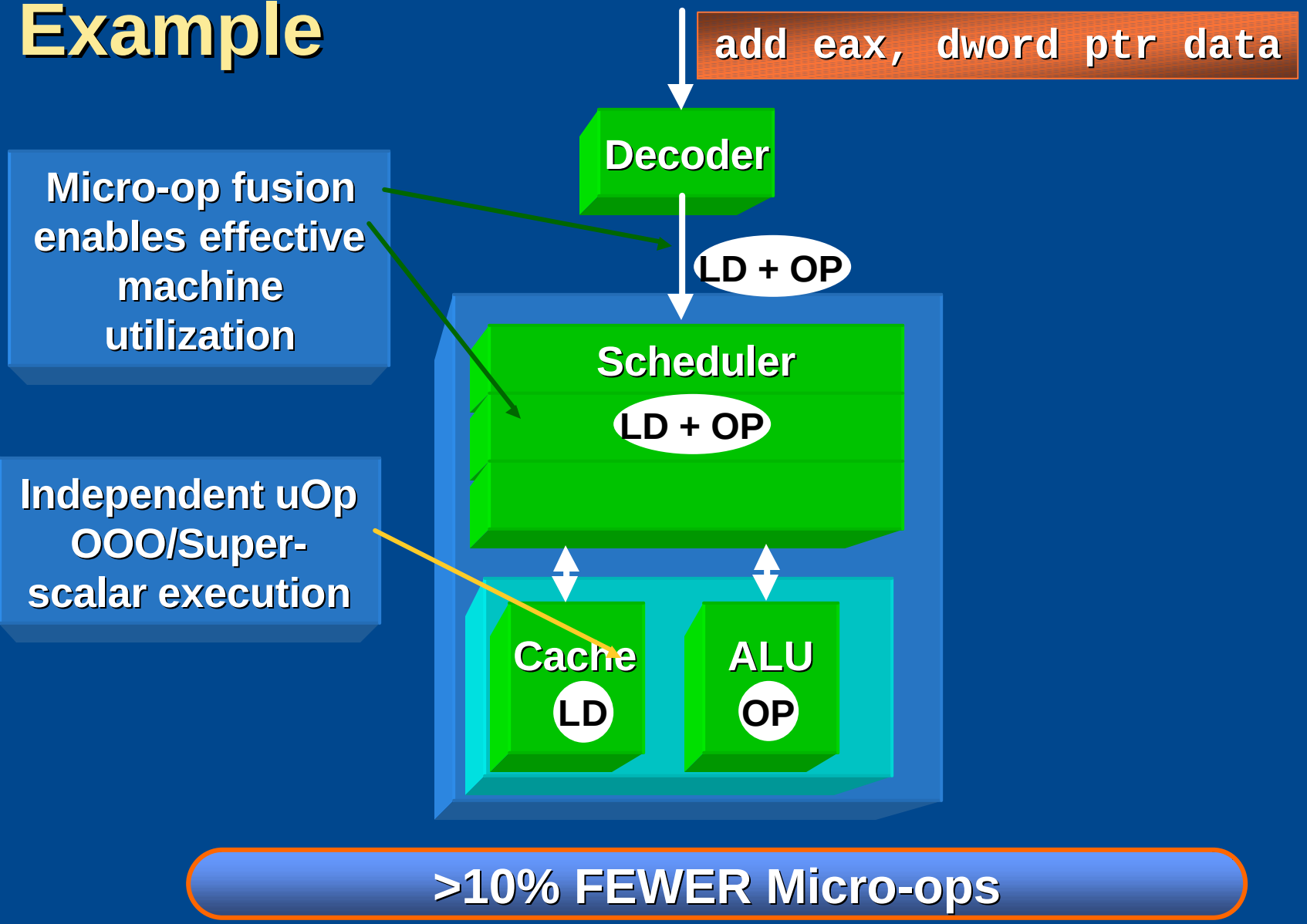


Example
Typical



Micro-Ops Fusion

Example

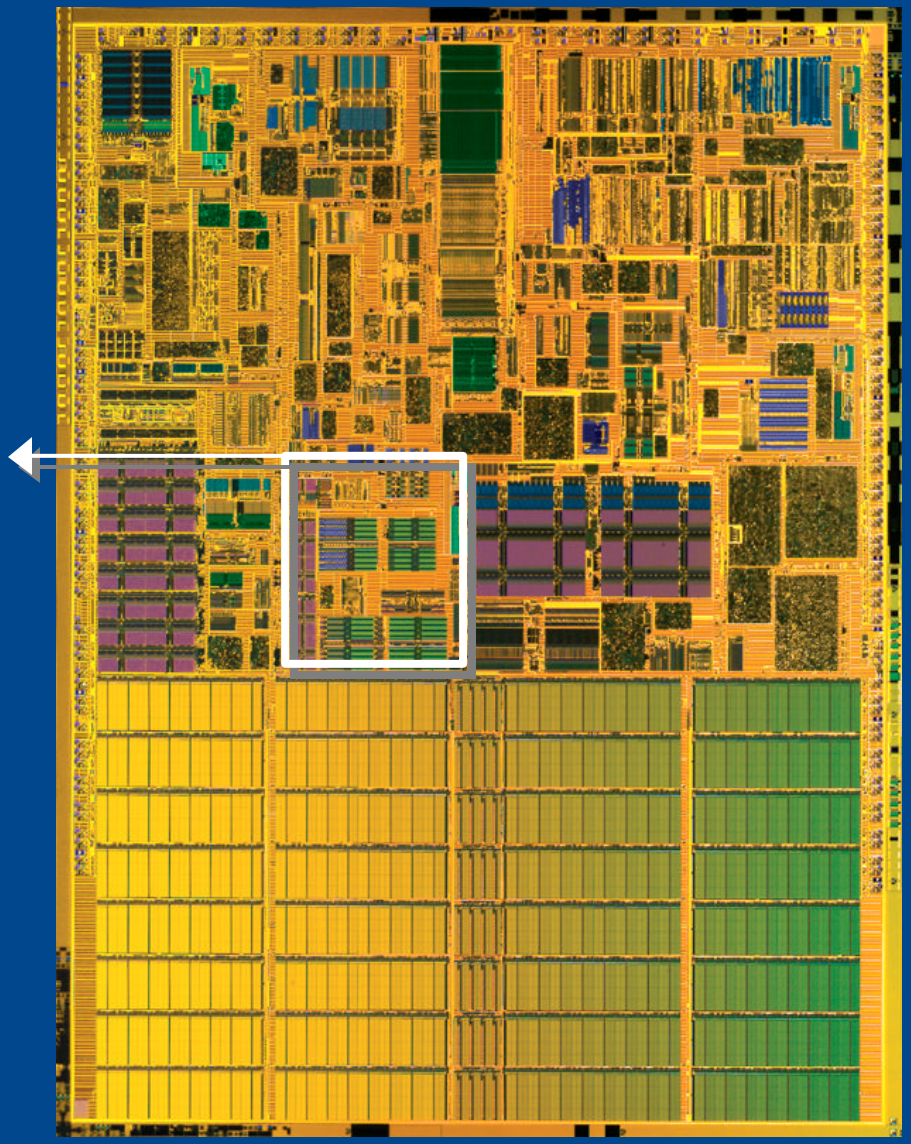


>10% FEWER Micro-ops

Intel Pentium M Processor

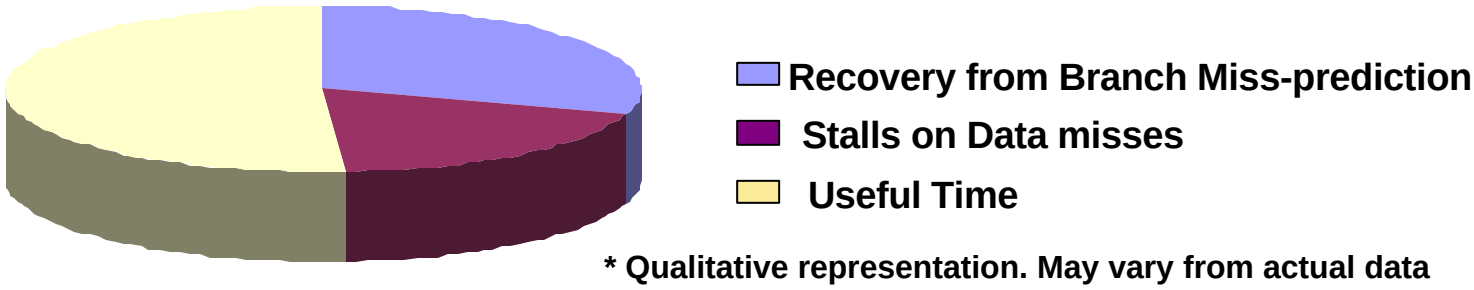
Micro-Ops Fusion fuses operations together to enable faster execution of instructions at lower power

Advanced Branch Prediction



Branch Mis-Prediction

- Significant penalty on branch mis-prediction
  - Performance
  - Power



* Qualitative representation. May vary from actual data

Today's processors typical execution time breakdown

Advanced Branch Prediction

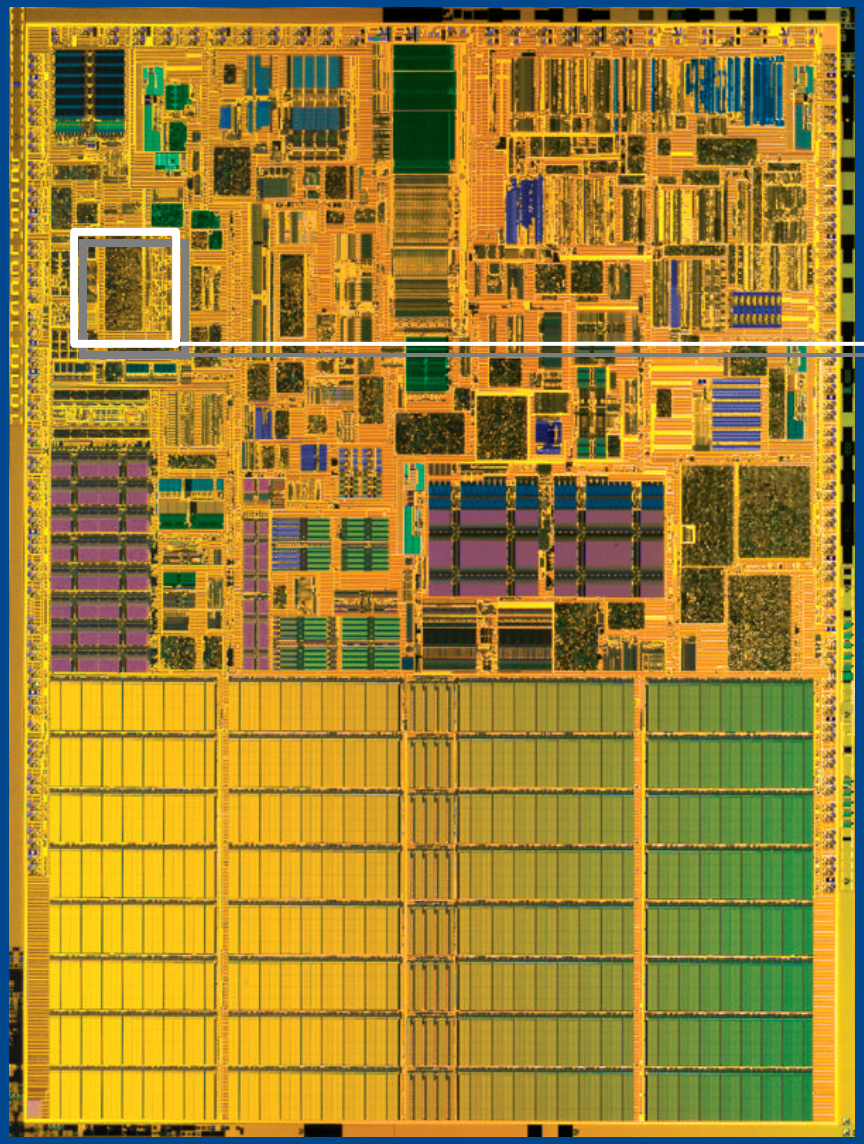
- Intel Pentium M processor employs best-in-class branch prediction
  - Captures all standard program behaviors
  - Enhanced support for newer programming paradigms
    - JIT and object oriented code
    - All sizes of iterational loops
- Intel Pentium M processor extends Bi-Modal/Global branch predictor
  - Loop detector
  - Indirect branch predictor

>20% FEWER branch mis-predictions

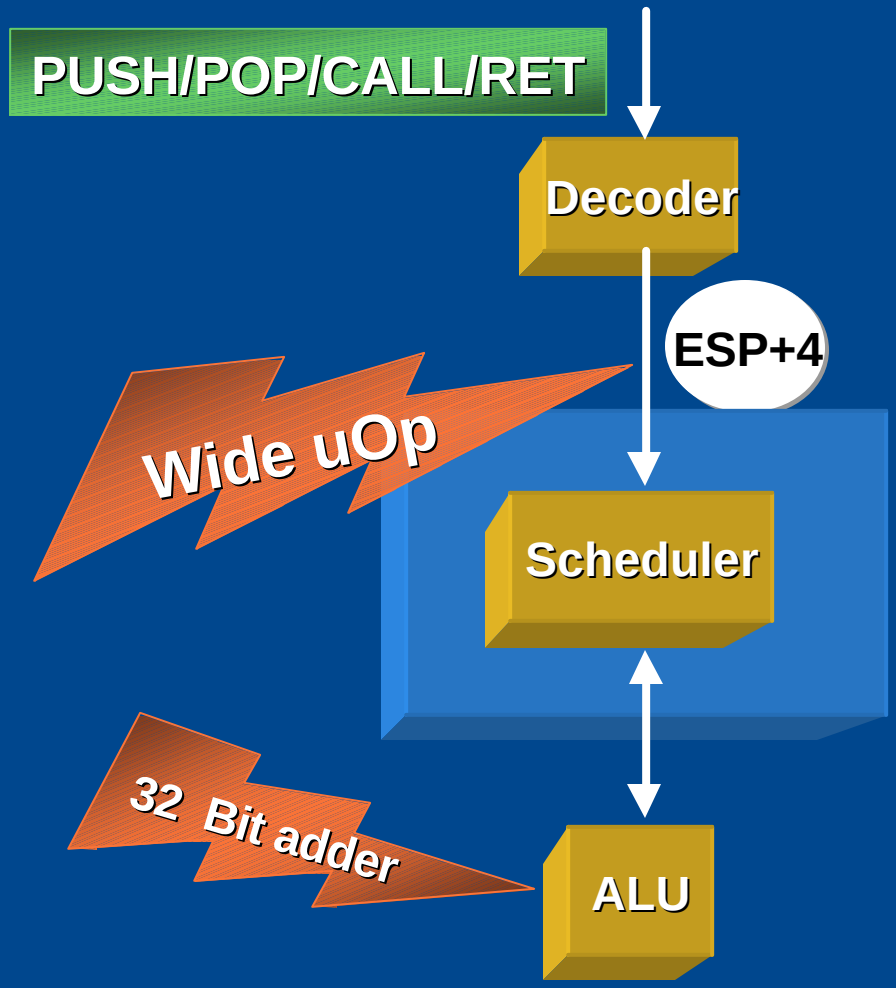
Intel Pentium M Processor

Micro-Ops Fusion
fuses operations together to enable faster execution of instructions at lower power

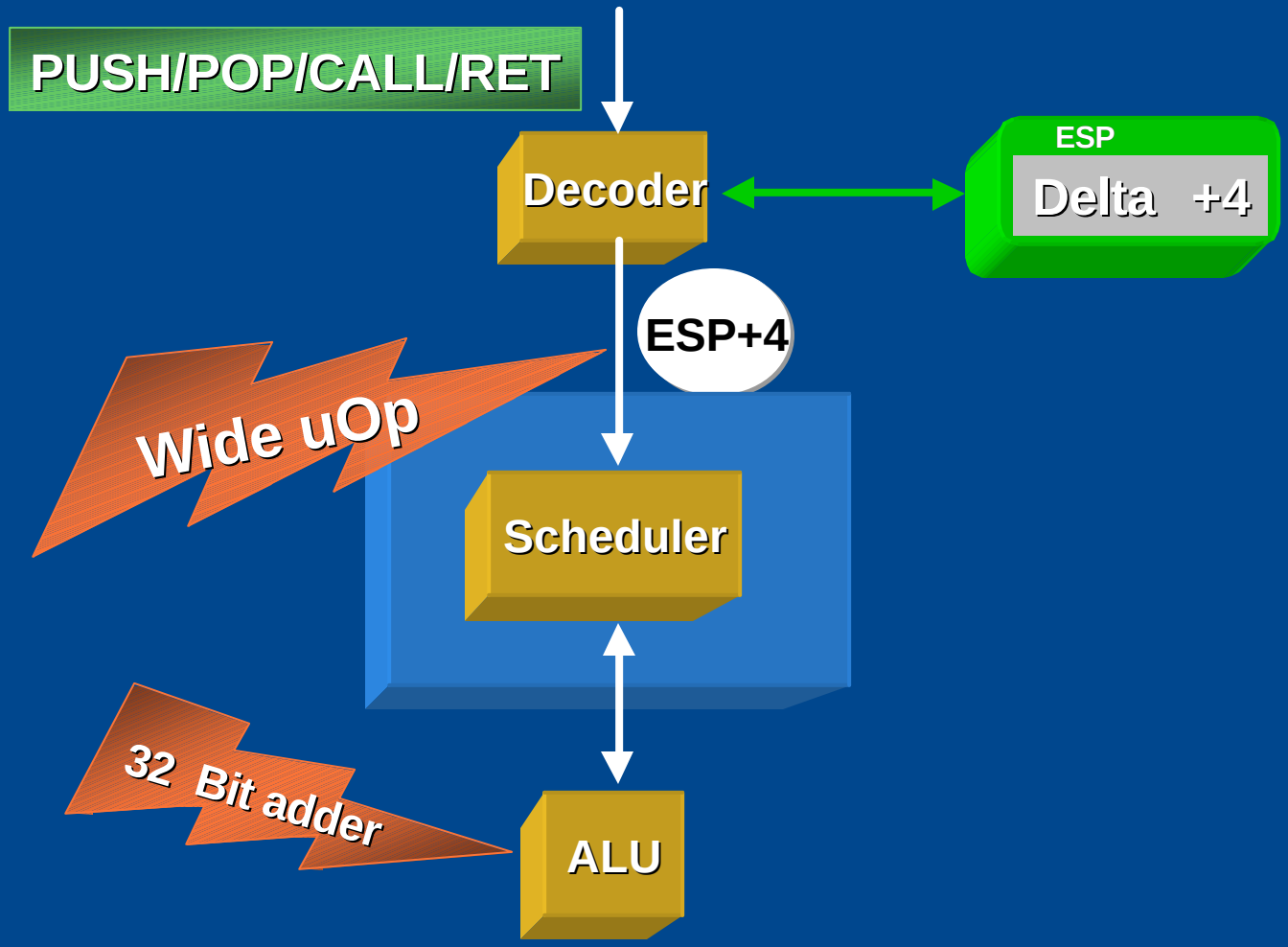
Advanced Branch Prediction
fewer re-dos for increased performance



Hardware Stack Manager



Hardware Stack Manager



>5% FEWER micro-ops

Intel Pentium M Processor

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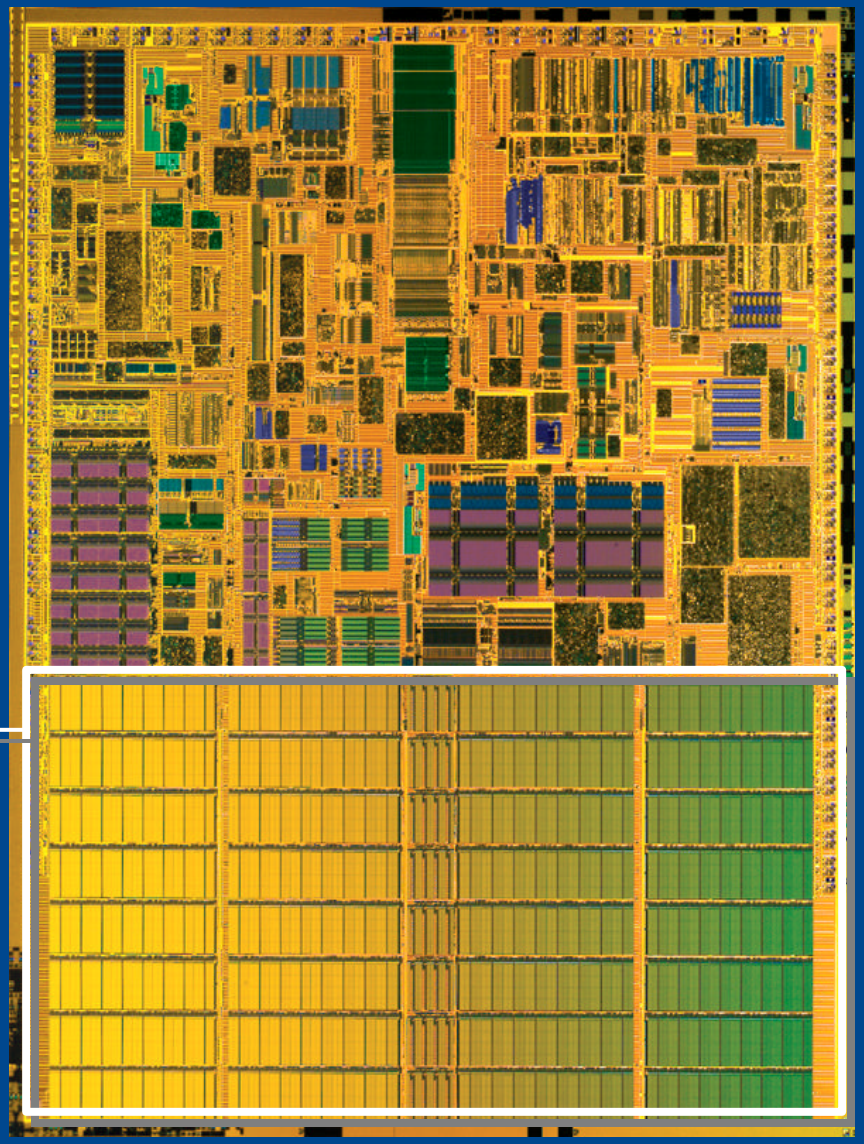
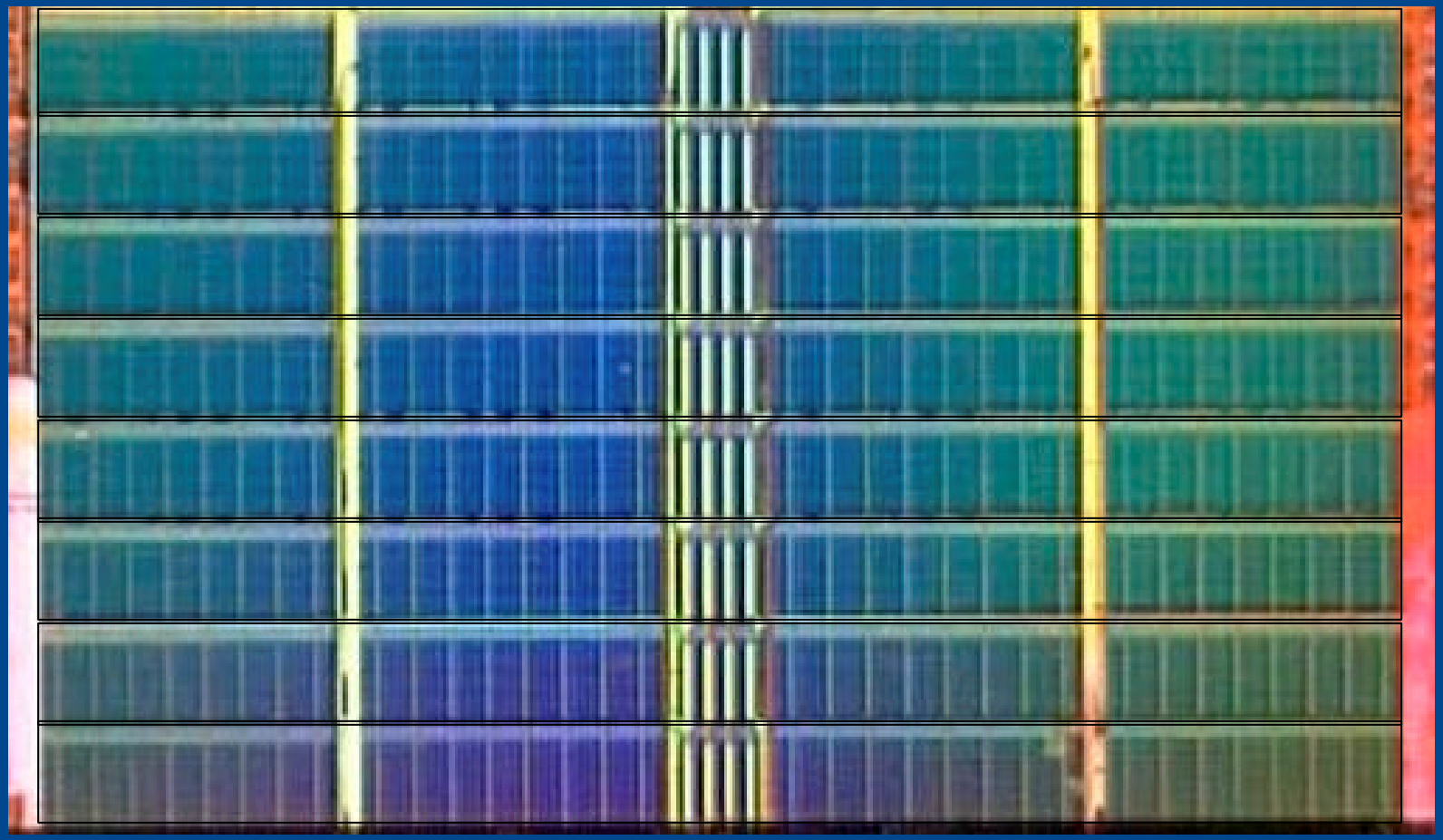
Advanced Branch Prediction
fewer re-dos for increased performance

1MB Power Optimized L2 Cache



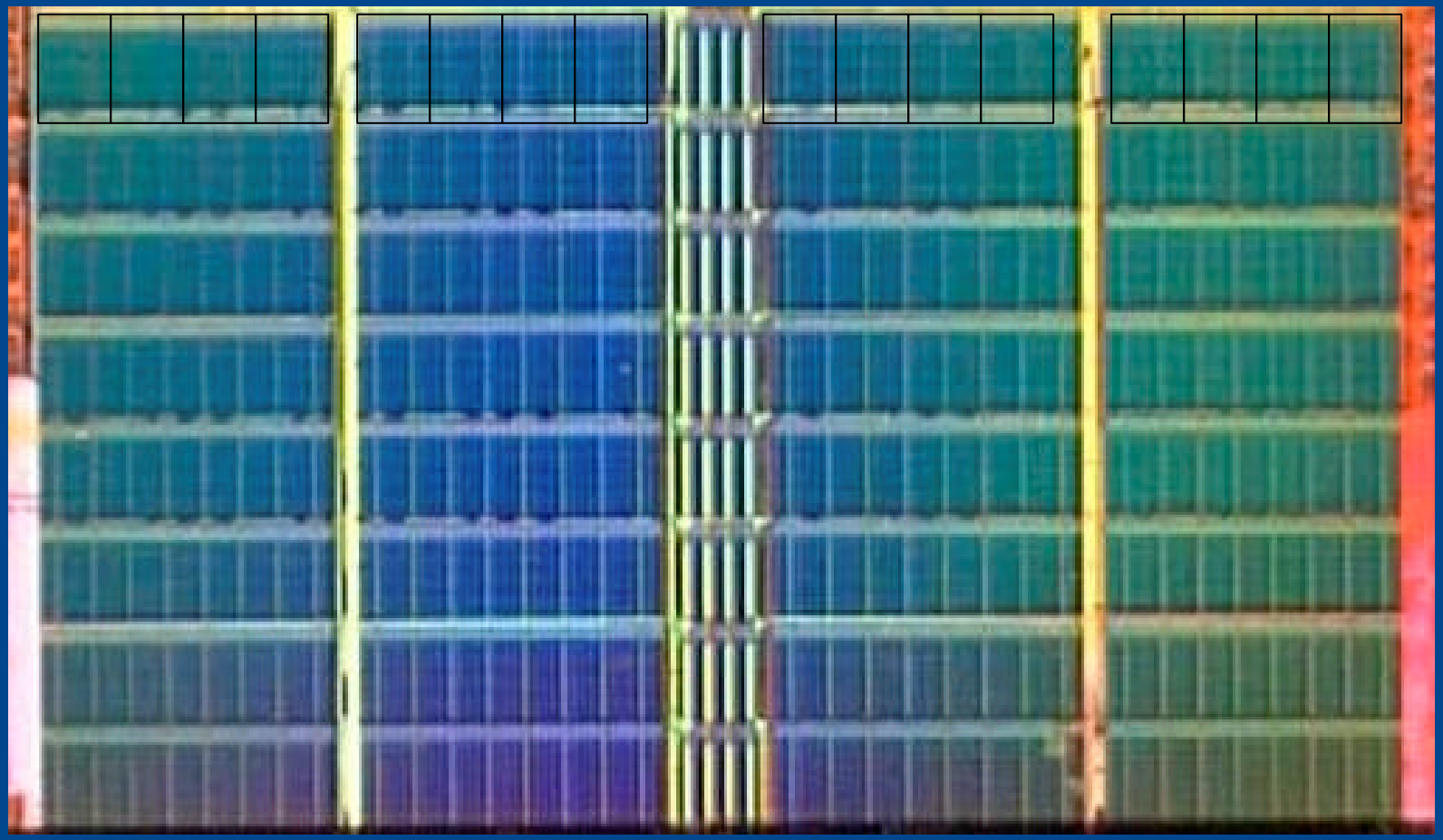
Dedicated Stack Management
faster instruction at lower power levels

Core/Cache Design



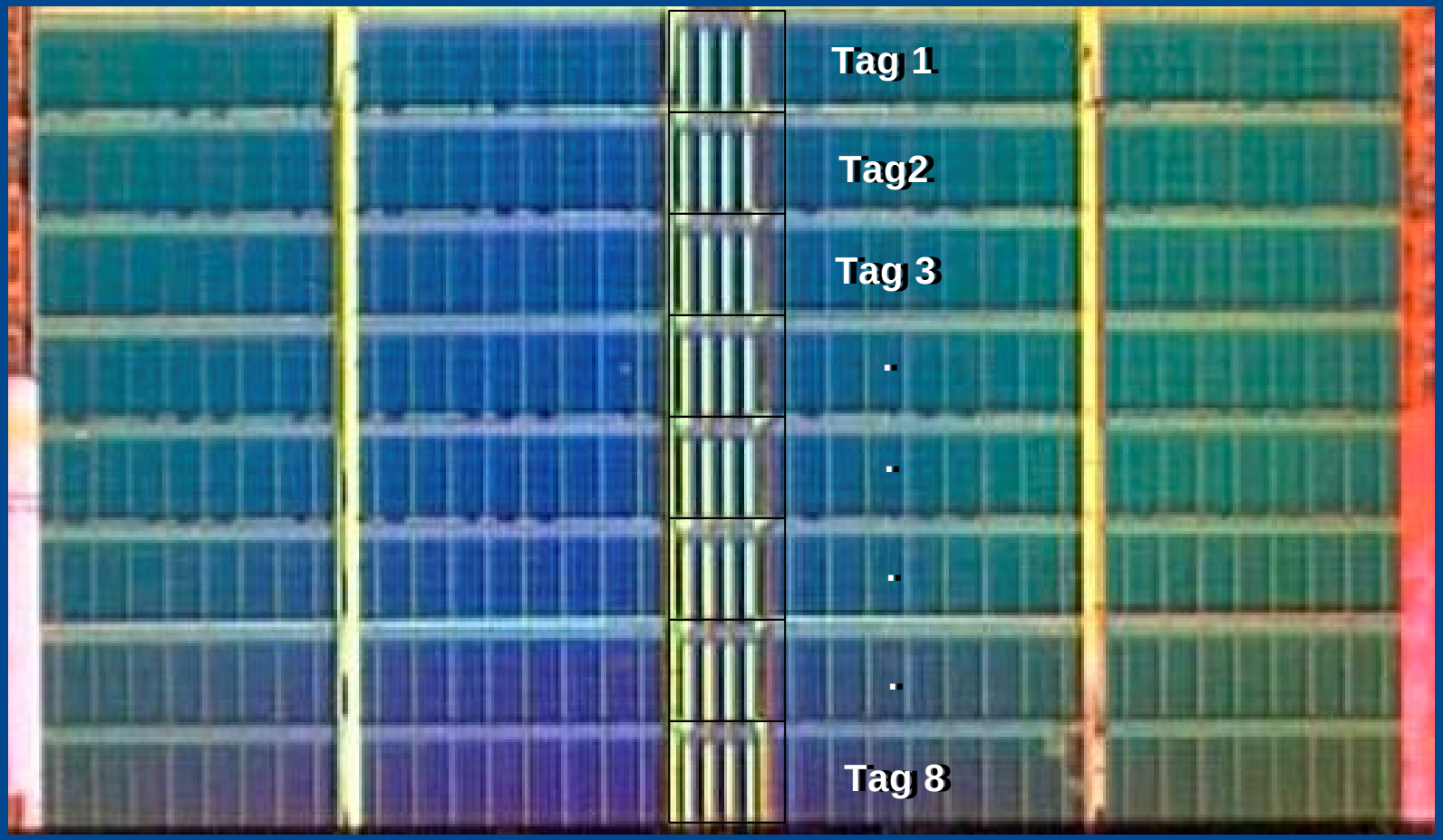
Eight ways set associative

Core/Cache Design



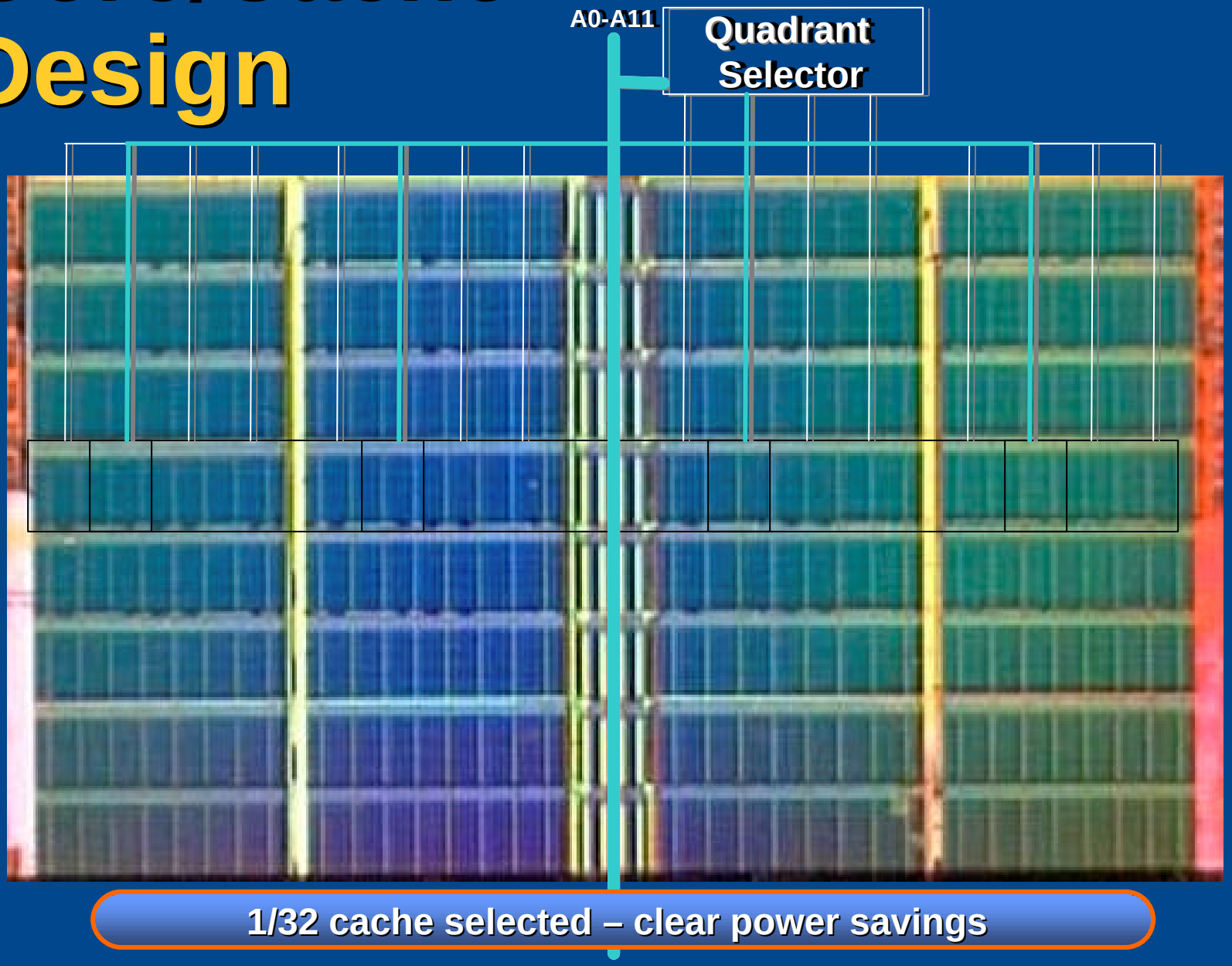
Four quadrants / way

Core/Cache Design



Centered Tag

Core/Cache Design



Intel Pentium M Processor

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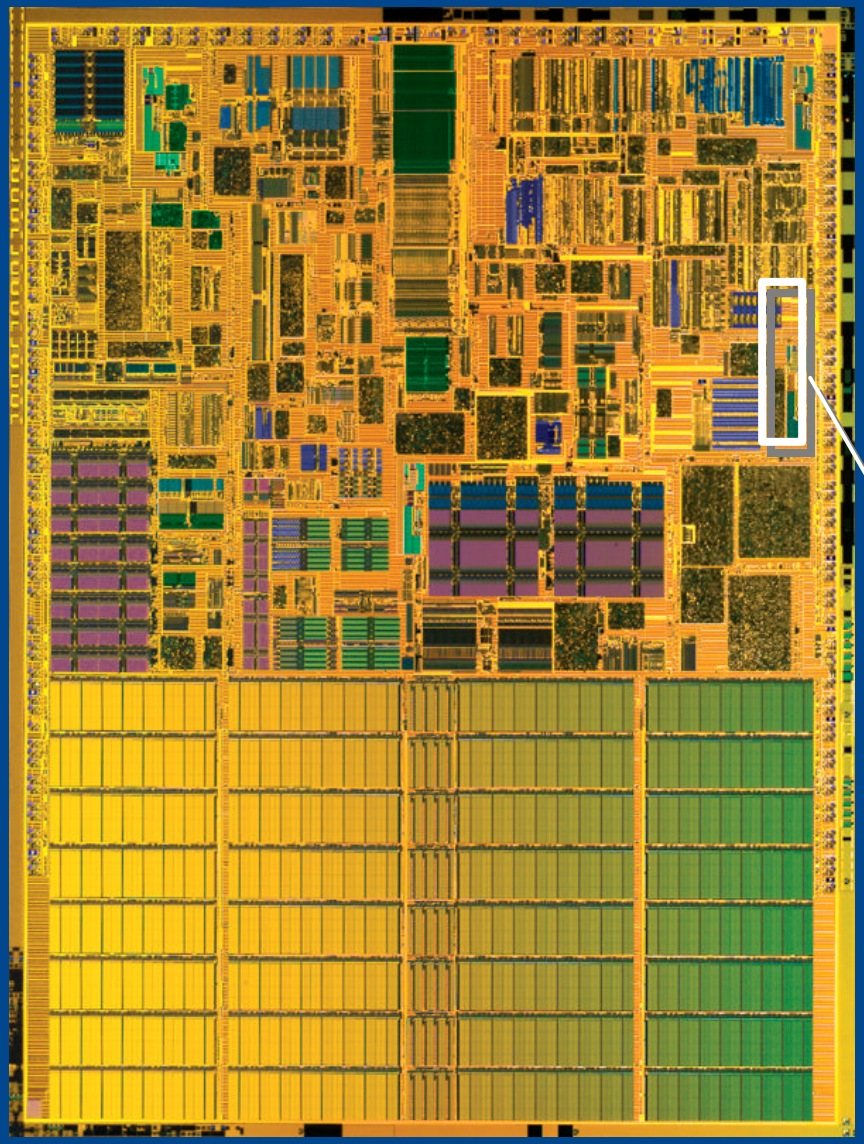
Advanced Branch Prediction
fewer re-dos for increased performance

1MB Power Optimized L2 Cache
enables higher CPU performance



Dedicated Stack Management
faster instruction at lower power levels

Enhanced Intel SpeedStep® Technology

Enhanced Intel Speedstep Technology

- Next-generation Intel processor performance control
  - Atomic transaction
  - Reduced unavailable processor time
  - Extends Voltage/Frequency benefits of Processor Performance Control to flexibility of multiple states
- Allows high-performance, low-power and additional adaptive operation modes
  - Windows® XP Native OS controlled
- Outstanding battery life and thermal management

Intel Pentium M Processor

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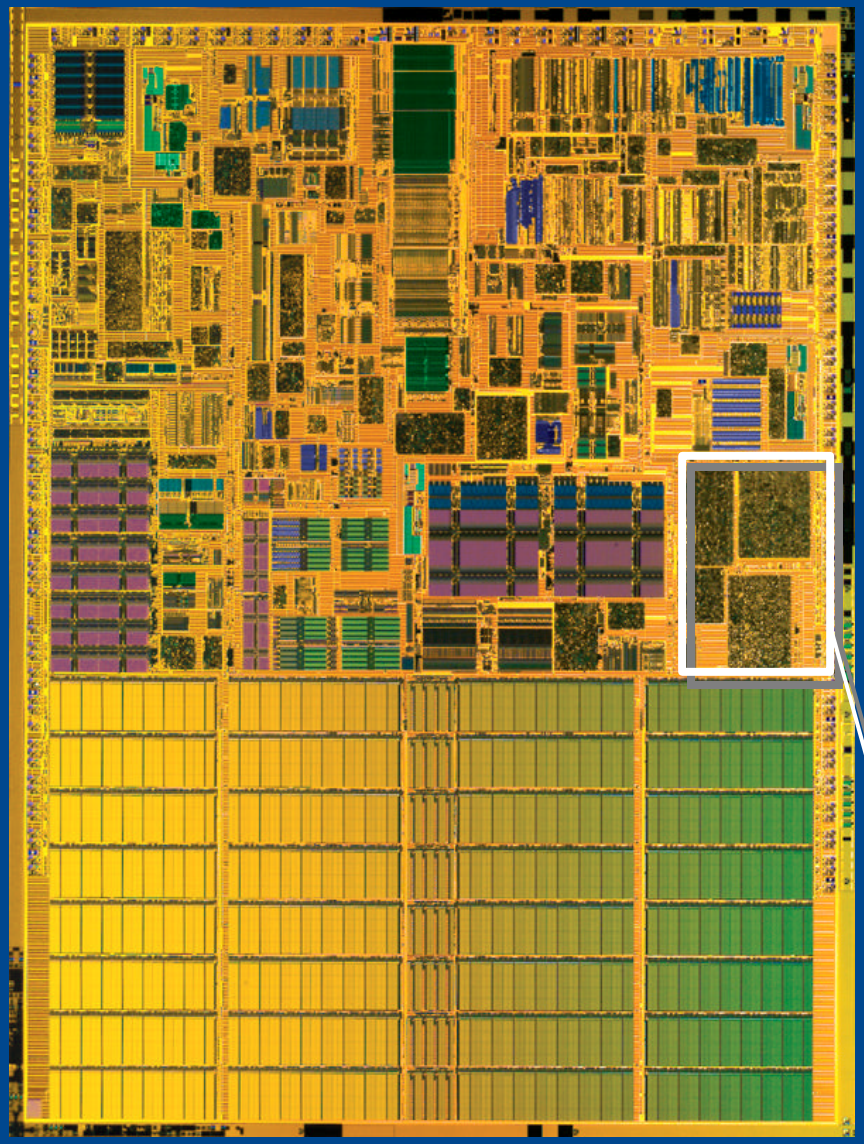

Dedicated Stack Management
faster instruction at lower power levels

Enhanced Intel SpeedStep® Technology
Multiple voltages and frequency operating points

400 MHz Power Optimized System Bus

Intel Pentium M Processor System Bus

- Desktop equivalent data rate
- Very low voltage
- Dynamic buffer control
- Dynamic on-die bus termination

High performance + power efficiency

Intel Pentium M Processor

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Advanced Branch Prediction
fewer re-dos for increased performance

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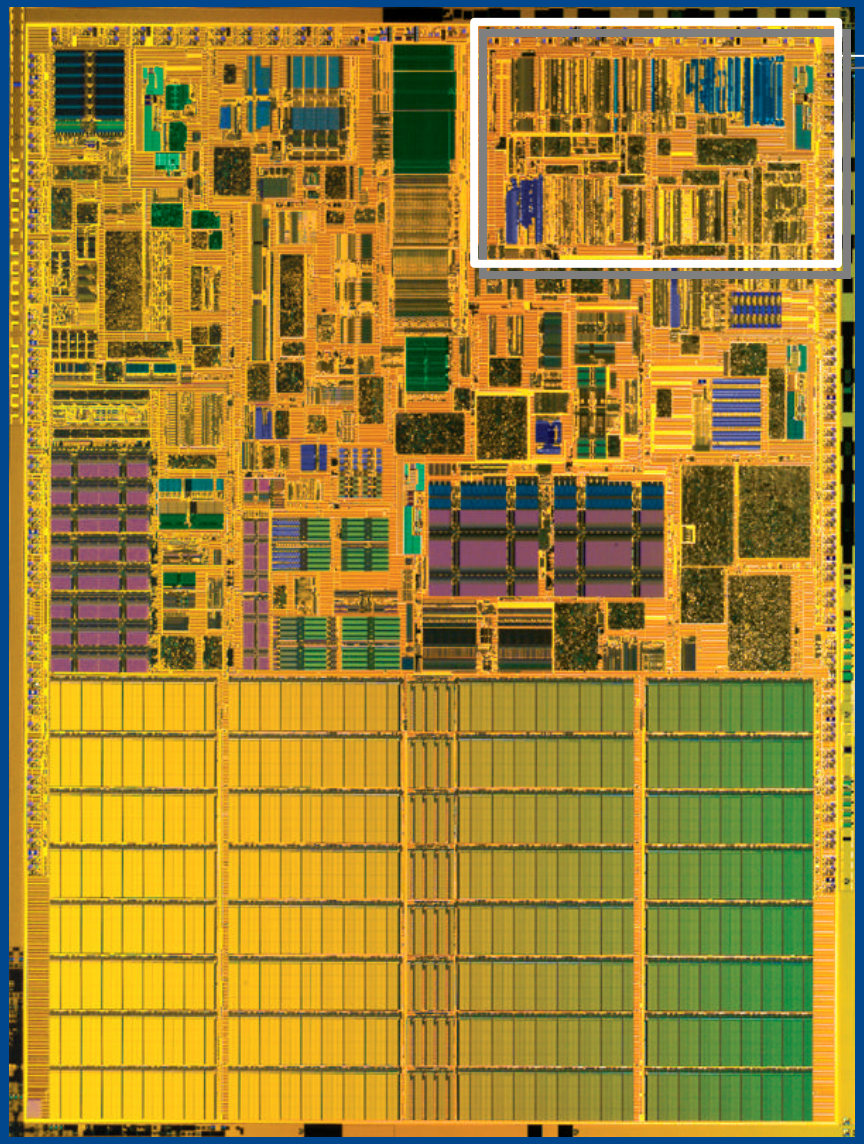
enables higher CPU performance



Streaming SIMD Extensions II
compatible with Pentium® 4 Processor optimized software

Dedicated Stack Management
faster instruction at lower power levels

Enhanced Intel SpeedStep® Technology
Multiple voltages and frequency operating points

400 MHz Power Optimized System Bus
faster system bus to enhance performance at lower power levels

Compatibility

- Streaming SIMD Extensions 2 (SSE2)
- Supports APIC mode
- Advanced debug capabilities
  - Easy monitoring of bus events via on-die logic analyzer trigger
  - Extended Power Management Debug hooks

Pentium® 4 Processor software compatibility

Software Optimizations
Performance

- Branching
  - Utilize the Advanced Branch prediction features of Intel Pentium M processor
    - E.G., Iterative loops
    - High-probability branch preceded by conditional branch
- Take advantage of Micro-ops fusion
  - Load/Execute typically fusible
  - Address store/data store typically fusible
- Intel enhanced Speedstep technology
  - No Timing dependencies on processor speed
    - Let OS manage processor performance

Software Optimizations
Power efficiency

- Do Not block PM features
  - Do not loop creating processor utilization - allow processor idle
  - Do not block Sx state entrance
  - Do not wake unnecessarily
    - Keep processor out of low power C states
- Be aware of OS PM messages
  - Self-manage for PM event
    - Handler for power broadcast messages
  - Be aware of when system is on DC
    - GetSystemPowerStatus
    - Tune to power schemes

Software Optimizations
Connectivity

- Multiple connect points possible
  - Do not fail functionality if connection lost
    - Allow access through any of connection points
- Unexpected disconnection
  - Utilize buffers
    - Allow continued operation when connection lost
    - Buffer used for recovery after connection re-established

Resources

- http://www.intel.com/design/mobile/index.htm?iid=ipp_mobiletech+deve&

Question And Answer